Abstract of the Disclosure

A serial bus controller using a nonvolatile ferroelectric memory is provided. The memory controller structure using a nonvolatile ferroelectric register enables control of variable access time according to addresses when data are exchanged through a serial bus. In the serial bus controller according to an embodiment of the present invention, access latency time by addresses is programmed using a nonvolatile ferroelectric register, and address access time is differently controlled depending on the programmed access latency when data are exchanged between a master and a FRAM chip through a serial bus, thereby improving system performance.